POWER-RAIL ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT WITH A DUAL TRIGGER DESIGN

ABSTRACT OF THE DISCLOSURE

A power-rail ESD (electrostatic discharge) protection circuit with a dual trigger design is proposed, which is coupled between a first power line and a second power line connected to an IC device for protecting the IC device against ESD on the first power line and the second power line. The proposed power-rail ESD protection circuit comprises a control circuit and at least one MOS device. The control circuit is coupled between the first power line and the second power line, and which is capable of, in the event of ESD in the first power line and the second power line, being triggered by the ESD to output a substrate-triggering voltage and a gate-driving voltage to the MOS device, causing the MOS device to bypass the ESD current from the first power line and the second power line. The circuit configuration of the proposed power-rail ESD protection circuit can help reduce the junction breakdown voltage in a MOS device and increase in ESD robustness.